TRH031M
13.56MHz Multi-Protocol Reader IC Guide

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Date	Version	Remark
2005. 5. 28	0.1	Preliminary
2005. 6. 25	1.0	1.0 version release
2005. 10. 16	2.0	Analog register map modify

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1 Product outlines, characteristics and advantages

TRH031M is 13.56MHz reader chip for contactless IC card reader applications. MCU Interface in TRH031M can use either Parallel Interface (8bit Address/Data Bus, 3bit Address bus) or Serial Interface supporting SPI. TRH031M supports multi-protocol (ISO 14443 Type A/B and ISO 15693).

ISO/IEC 14443 Type A and Type B and ISO/IEC 15693 standards consist of 4 separate Parts. TRH031M supports all four parts of above three ISO standards.

Part 1 : Physical Characteristics

This part of ISO/IEC 14443 specifies the physical characteristics of proximity cards (PICC). It applies to identification cards of the card type ID-1 operating in proximity of a coupling device.

Part 2 : Radio Frequency power and signal interface

This part of ISO/IEC 14443 specifies the characteristics of the fields to be provided for power and bi-directional communication between proximity coupling devices (PCDs) and proximity cards (PICCs).

This part of ISO/IEC 14443 does not specify the means of generating coupling fields, nor the means of compliance with electromagnetic radiation and human exposure regulations which can vary according to country.

Part 3 : Initialization and anti-collision

This part of ISO/IEC 14443 describes:

- Polling for proximity cards (PICCs) entering the field of a proximity coupling device (PCD);
- The byte format, the frames and timing used during the initial phase of communication between PCDs and PICCs;
- The initial Request and Answer to Request command content;
- Methods to detect and communicate with one PICC among several PICCs (anti-collision);
- Other parameters required to initialize communications between a PICC and PCD;
- Optional means to ease and speed up the selection of one PICC among several PICCs based on application criteria.

Protocol and commands used by higher layers and by applications and which are used after the initial phase are described in ISO/IEC 14443-4.

Part 4 : communication Transmission Protocol

This part of ISO/IEC 14443 specifies a half-duplex block transmission protocol featuring the special needs of a contactless environment and defines the activation and deactivation sequence of the protocol.

For ISO 15693, it as internal 8 bit timer and 64 byte FIFO. This FIFO send/receive signals. In addition, when RESET is set to HIGH, there is virtually no current waste other than Leakage current in nA unit while chip POWER DOWN.

TRH031M supports voltage from 2.7V to 3.6V, and there is not much difference in distance recognition based on voltage. However, card recognition range is narrowed when voltage is lower.

2 Block Diagram and Pin Organization Chart

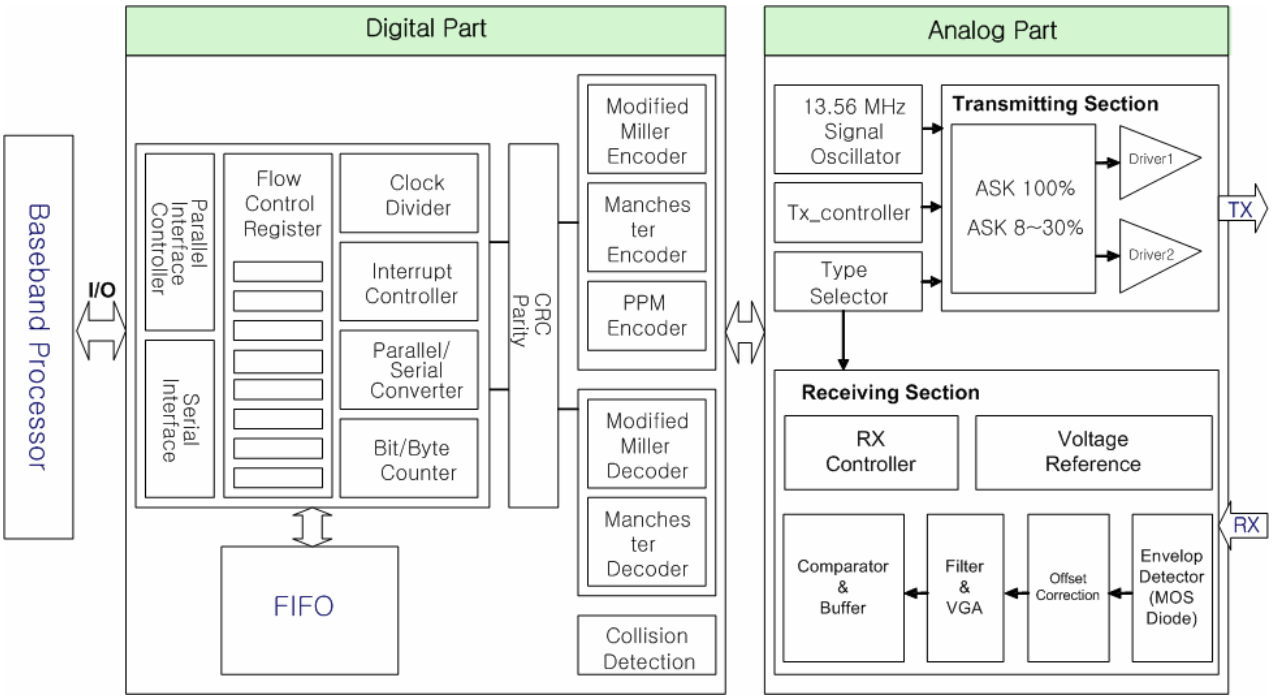

Figure1. TRH031M Block Diagram

TRH031M is divided largely into two parts.

Analog Part includes antenna driver circuit, transmit block (altered data transmission to card) and receiver block (card response recognition).

Digital Part includes Miller, Manchester Encoder/Decoder, parity, CRC processing logic, Timer, FIFO, MCU Interface and Protocol processing.

TRH031M works without external Amp upto 120mA by generating maximum TX driver from antenna.

TRH031M Pin Organization Chart

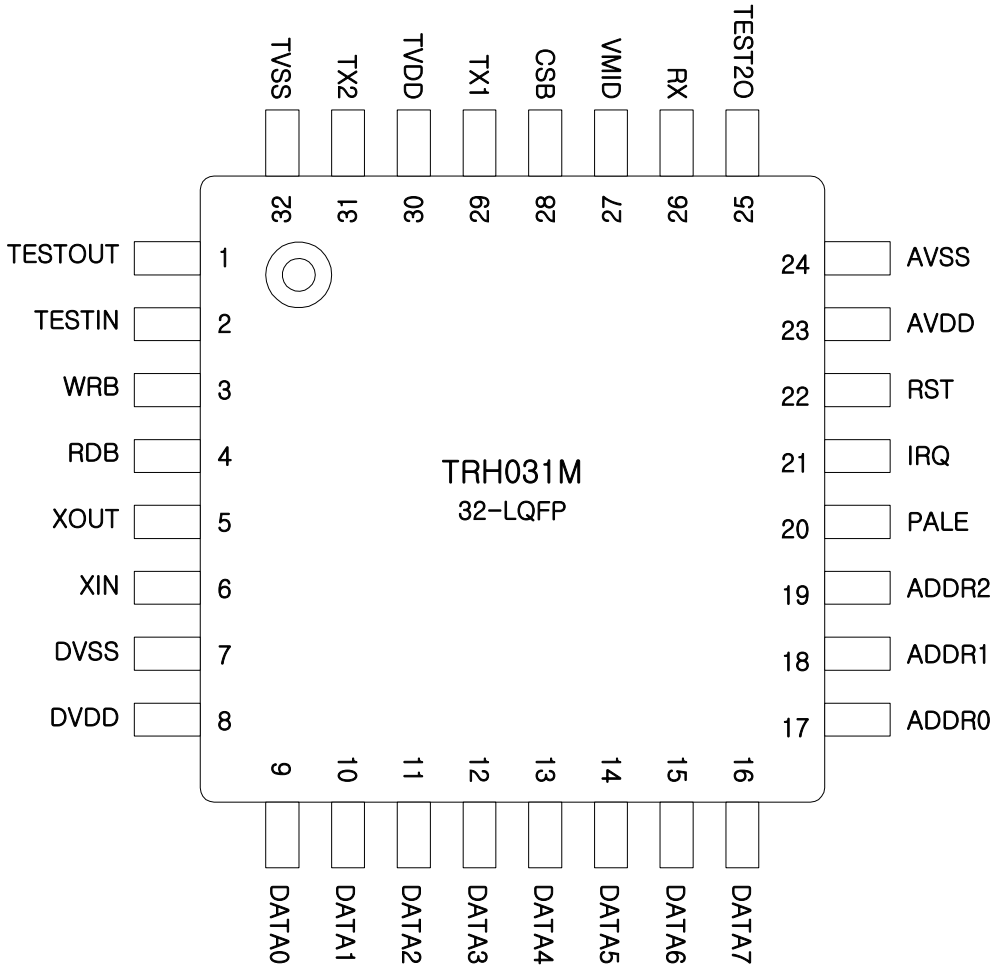

Figure2. TRH031M pin map

3 PIN DESCRIPTIONS

Pin Name	Type	Pin Description	Number
TX1	O	Transmitter 1:delivers the modulated 13.56MHz energy carrier	29
TX2	O	Transmitter 2;delivers the modulated 13.56MHz energy carrier	31
CSB	I	Chip Select signal	28
WRB	I	Not Write: strobe to write data(applied on DATA0 to DATA7)	3
R/NW	I	Read Not Write: selects if a read or write cycle shall be performed.	
RDB	I	Not Read: strobe to read data (applied on DATA0 to DATA7)	4
NDS	I	Not Data Strobe: strobe for the read and the write cycle	
PALE	I	Address Latch Enable : strobe signal to latch DATA0 to DATA5 into the internal address latch when HIGH	20
ADDR0	I	Address Line 1: Bit 0 of register address	17
ADDR1	I	Address Line 1: bit 1 of register address	18
ADDR2	I	Address Line 2: bit 2 of register address	19
RX	I	Receiver Input: Input pin for the cards response, which is the load modulated 13.56MHz energy carried that is coupled out from the antenna circuit.	26
RST	I	Reset and Power Down: When HIGH, internal current sinks are switched off, the oscillator is inhibited, and the input pads are disconnected from the outside world. With a negative edge on this pin the internal reset phase	22
XIN	I	13.56MHz Crystal Oscillator Input	6
XOUT	O	Crystal Oscillator Output: Output of the inverting amplifier of the oscillator.	5
IRQ	O	Interrupt Request: output to signal an interrupt event	21
TEST2O	O	Auxiliary Output: This pin delivers analog test signals. Used for factory test	25
TESTIN	I	Used at Factory Test	2
TEST1O	O	Used at Factory Test	1
VMID	PWR	Internal reference voltage: This pin delivers the internal reference voltage. Note: It has to be supported by means of a 100 nF block capacitor.	27
TVDD	PWR	Transmitter Power Supply; supplies the output stages of TX1 and TX2	30
TVSS	PWR	Transmitter Ground: supplies the output stage of TX1 and TX2	32
DVDD	PWR	Digital Power Supply	8
DVSS	PWR	Digital Ground	7
AVDD	PWR	Analog Power Supply	23
AVSS	PWR	Analog Ground	24
DATA7 – DATA0	I/O	8-tib Bidirectional Data Bus(Dedicated Address Bus Mode) or Address/Data bus(Multiplexed Address Bus Mode)	16 - 9

4 Electric Characteristics

Absolute maximum ratings

Symbol	Parameter	MIN	MAX	UNIT
T_{amb}, T_{sto}	Ambient or storage temperature range	-45	+150	℃
DVDD AVDD TVDD	DC Power supply	-0.5	4.0	V
V_{in}	Absolute voltage on any digital pin to DVSS	-0.5	DVDD+0.3	V
V_{RX}	Absolute voltage on RX pin to AVSS	-0.5	AVDD+0.3	V

Operating condition range

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
T_{amb}	Ambient or storage temperature range	-	-25	+25	+85	℃
DVDD	Digital Power supply	DVSS=AVSS=TVSS=0V	2.7	3.0	3.6	V
AVDD	Analog Power supply	DVSS=AVSS=TVSS=0V	2.7	3.0	3.6	V
TVDD	Transmitter Power supply	DVSS=AVSS=TVSS=0V	2.7	3.0	3.6	V

Current consumption

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
I_{DVDD}	Digital Supply current	Idle Command	3.0	3.8	5.8	mA
		Soft Power Down mode	-	0.1	1	uA
		Hard Power Down mode	-	0.1	1	uA
I_{AVDD}	Analog Supply current	Idle Command, Receiver On	1.7	2.2	2.4	mA
		Power Down mode	-	0.01	0.03	uA
I_{TVDD}	Transmitter Supply current	Continuous Wave Antenna unconnected	130	150	180	mA
		TX1 and TX2 unconnected, TX1,2 disable / clock on	6	7	10	uA
		TX1 and TX2 unconnected, TX1,2 disable / clock off	-	0.05	0.10	uA

Standard input pin characteristics

Symbol	Parameter	Conditions	MIN	MAX	UNIT
I_{leak}	Input Leakage Current	-	-1.0	+1.0	uA
V_T	Threshold	DVDD < 3.0 V	0.35DVDD	0.65DVDD	V

※ DATA0 to DATA7, ADDR0, ADDR1 have CMOS input characteristics.

Schmitt trigger input pin characteristics

Symbol	Parameter	Conditions	MIN	MAX	UNIT
I_{leak}	Input Leakage Current	-	-1.0	+1.0	uA
V_{T+}	Positive-Going Threshold	DVDD < 3.0 V	0.35DVDD	0.65DVDD	V
V_{T-}	Negative-Going Threshold	DVDD < 3.0 V	0.35DVDD	0.65DVDD	V

※ CSB, WRB, RDB, PALE, TESTIN have Schmitt-Trigger characteristics.

5 Analog Offchip component & Register setting

TRH031M Analog Off chip component

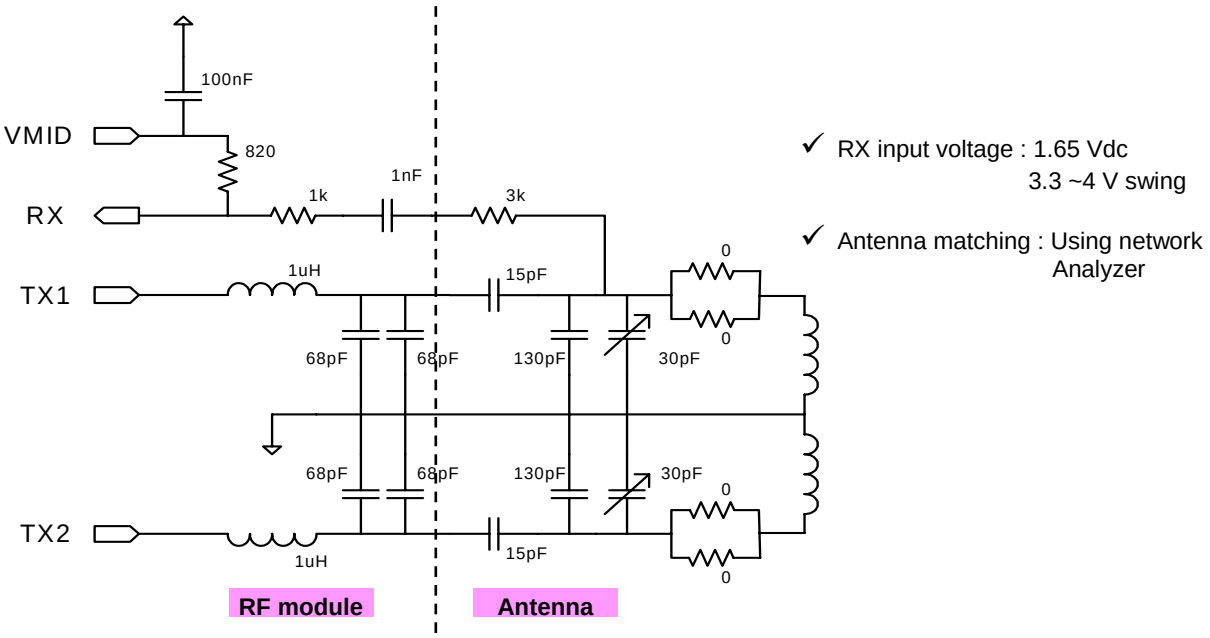

Figure3. TRH031M Analog Off chip component

TRH031M Analog Control Register

Addr	Name	Description	Value							
			7	6	5	4	3	2	1	0
0x11	TxControl	Antenna driver pins control	0	Modulator source		ASK 100	TX2 inv	TX2 NMd	TX2 en	TX1 en
0x12	CwConduct.	Antenna driver pins conductance	0	0	CwConductance					
0x13	ModConduct.	Modulation conductance	0	0	ModConductance					
0x19	RxControl	Receiver & VGA gain control	0	0	0	0	0	VGA Gain		
0x1C	RxThreshold	Comparator reference voltage / Hysteresis range control	0	0	Hysteresis Range			Comparator Ref. voltage		

TRH031M Register Setting Value by Communication Mode

ADDR	NAME	A-Type Value	B-Type Value	15693 Value
11H	TXCONTROL	5BH	4BH	5BH
12H	CWCONDUCT	3FH	3FH	3FH
13H	MODCONDUCT	X	03H	X
14H	CODCONT	01H	20H	2FH
15H	MODWIDTH	10H	X	X
19H	RXCONTROL1	03H	03H	03H
1AH	DECODCONT	08H	18H	10H
1CH	RXTHRESHOLD	18H	18H	18H
1EH	RXCONTROL2	81H	X	X
21H	RXWAIT	06H	0BH	06H

(X : Don't Care)

From above 19 and 1C registers that determine demodulation performance in receiver level must be handled with utmost caution. Recommended setting values are 03H and 18H, however, based on reader module noise environment maximum from 04H/18H up to 04H/20H, 03H/18H, 03H/20H & 02H/18H are possible. Increasing Gain and decreasing Hysteresis range will enhance performance of demodulation, therefore, increasing card reading range. However, it will become volatile to noise. Therefore, we do not recommend maximum Gain in register setting. (19H : 05H)

6 PACKAGE DIMENSIONS

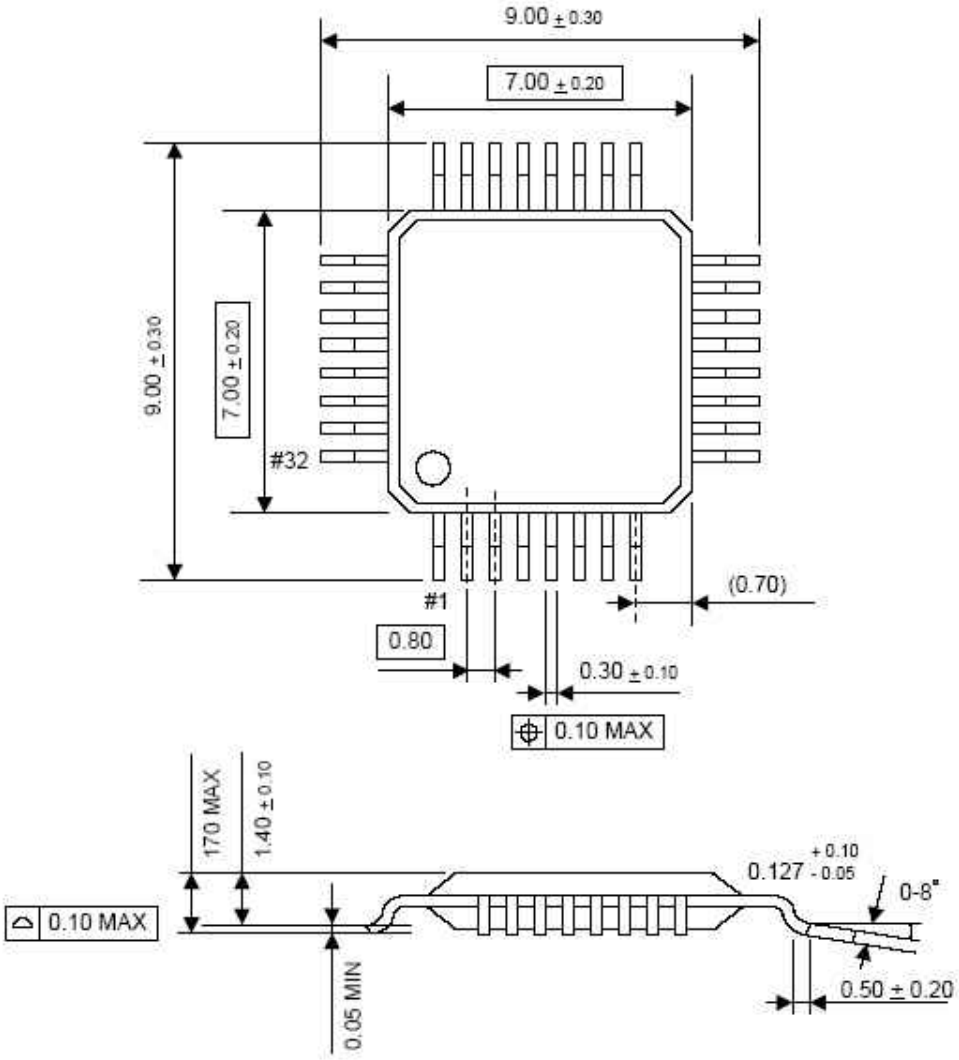

Figure4. 32-pin LQFP Package Dimension